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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/690,859	10/22/2003	Chien-Mao Liao	10113101	6925

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EXAMINER	
LE, THAO P	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 02/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

CT

Office Action Summary	Application No.	Applicant(s)	
	10/690,859	LIAO ET AL.	
	Examiner	Art Unit	
	Thao P. Le	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10/22/03* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Acknowledge is made of applicants' claim for foreign priority base on an application 92120043 filed in Japan on 07/23/2003.

It is noted that Applicants have filled a certified copy of said application as required by U.S.C 119, which papers have been placed of record in the file.

2. Claims 1-48 are pending.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-4, 6-9, 10-12, 15-17 are rejected under 35 USC 102 (a) as being anticipated by Hong et al., U.S. Patent No. 6,566,229.

Regarding claim 1, Hong et al. discloses a method of forming a trench isolation similar to what recited in claim 1 (See Figs. 1-5 and Cols. 1-8), the method comprising:

. providing a semiconductor substrate 10 with a trench 19 wherein the substrate has a mask layer (line 49, Col. 3);

. forming a first insulating layer 21 to cover the substrate and the trench wherein the trench is filled with the first insulating layer (fig. 2);

. anisotropically etching the first insulating layer (lines 65-67, Col. 4) to below the level of the semiconductor substrate (211, fig. 3);

. forming a second insulating layer 31 to cover the substrate and the trench, and planarizing the second insulating layer to expose the mask layer (lines 25-28, Col. 5).

Regarding claim 2, Hong et al. discloses the mask layer is a nitride layer (lines 28-29, Col. 5).

Regarding claim 3, Hong et al. discloses the first insulating layer is an oxide layer (Cols. 3-4).

Regarding claim 4, Hong et al. discloses in prior art that oxide layer can be formed using LPCVD.

Regarding claim 6, Hong et al. discloses the first insulating layer is lower than the semiconductor substrate by about 1000 A (at least 300 A) after anisotropic etching (line 65, Col. 4).

Regarding claim 7, Hong et al. discloses the second insulating layer is an oxide layer (line 19, Col. 5).

Regarding claim 8, Hong et al. discloses the second oxide layer is TEOS oxide layer (lines 8-11, Col. 3).

Regarding claim 9, Hong et al. discloses wherein the planarizing is chemical mechanical polishing (lines 25-26, Col. 5).

Regarding claim 10, Hong et al. discloses a method of forming a trench isolation similar to what recited in claim 10 (See Figs. 1-5 and Cols. 1-8), the method comprising:

. providing a semiconductor substrate 10, wherein a pad layer 11, a mask layer (line 47, col. 3), and a patterned photoresist layer (not shown, line 49, Col. 3) with an opening are formed thereon;

. etching the mask layer, the pad layer, and the substrate to form a trench 19 using patterned photoresist layer as a mask (lines 50-53, Col. 3);

. removing the patterned photoresist layer (Fig. 1);

. forming an oxide layer 21 to cover the substrate and the trench wherein the trench is filled with the first insulating layer (fig. 2), the oxide layer can be formed using LPCVD (Cols. 1-2);

. anisotropically etching the first insulating layer (lines 65-67, Col. 4) to below the level of the semiconductor substrate (211, fig. 3) by at least 300 A (about 1000 A; line 65, Col. 4);

. forming an insulating layer 31 to cover the substrate and the trench, and planarizing the second insulating layer to expose the mask layer (lines 25-28, Col. 5);

. removing the mask layer (Fig. 5).

Regarding claim 11, Hong et al. discloses wherein the pad layer is an oxide layer.

Regarding claim 12, Hong et al. discloses the mask layer is a nitride layer (lines 28-29, Col. 5).

Regarding claim 15, Hong et al. discloses the first insulating layer is an oxide layer (Cols. 3-4).

Regarding claim 16, Hong et al. discloses the second oxide layer is TEOS oxide layer (lines 8-11, Col. 3).

Regarding claim 17, Hong et al. discloses wherein the planarizing is chemical mechanical polishing (lines 25-26, Col. 5).

6. Claims 5, 14 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Hong et al., U.S. Patent No. 6,566,229.

Regarding claims 5, 14, Hong et al. discloses the etching process can be anisotropic etching but fails to specify that the anisotropic etching is plasma or reactive

ion etching. It would have been well known in the art that plasma or reactive ion etching is one type of anisotropic etching.

7. **Claim 13 is rejected under 35 U.S.C. 103 (a) as being unpatentable over Hong et al., U.S. Patent No. 6,566,229, in view of Hong et al., U.S. Patent No. 6,593,207.**

Regarding claim 13, Hong et al., U.S. Patent No. 6,566,229 doesn't mention the aspect ratio of the trench is greater than 6, however, Hong et al., U.S. Patent No. 6,593,207 discloses that the aspect ratio of the trench is 4 or higher (lines 42-43, Col. 4). It would have been obvious to one having ordinary skill in the art at the time the invention was made to have high aspect ratio is greater than 6 because when the high aspect ratio is high, the trench is not able to be filled in one step for forming a device isolation but two steps are required as disclosed in Hong et al. and present invention.

8. Claims 18-26, 27-29, 31-35 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Hong et al., U.S. Patent No. 6,566,229, in view of Lin et al., U.S. patent No. 6,713,365.

. providing a semiconductor substrate 10 with a trench 19 wherein the substrate has a mask layer (line 49, Col. 3);

. forming a first insulating layer 21 to cover the substrate and the trench wherein the trench is filled with the first insulating layer (fig. 2);

. anisotropically etching the first insulating layer (lines 65-67, Col. 4) to below the level of the semiconductor substrate (211, fig. 3);

. forming a second insulating layer 31 to cover the substrate and the trench, and planarizing the second insulating layer to expose the mask layer (lines 25-28, Col. 5).

Hong et al. fails to disclose the formation of spacer on a sidewall of the trench by etching the first insulating layer.

Lin et al. discloses the method of filling trench isolation similar to Hong et al. and further discloses the formation of spacer on a sidewall of the trench by etching the first insulating layer. It would have been obvious to one having ordinary skill in the art at the time the invention was made to etch the first insulating layer as disclosed in Hong et al. or a spacer as disclosed in Lin et al. because the functions and manners of the device would not make any different in the method of forming trench isolation having high aspect ratio using two steps of filling the trench.

Regarding claim 19, Hong et al. discloses the mask layer is a nitride layer (lines 28-29, Col. 5).

Regarding claim 20, Hong et al. discloses the first insulating layer is an oxide layer (Cols. 3-4).

Regarding claim 21, Hong et al. discloses in prior art that oxide layer can be formed using LPCVD.

Regarding claim 22, Hong et al. discloses the first insulating layer is lower than the semiconductor substrate by about 1000 A (at least 300 A) after anisotropic etching (line 65, Col. 4).

Regarding claim 23, Hong et al. discloses that after etching, the first insulating layer is lower than the substrate.

Regarding claim 24, Hong et al. discloses the second insulating layer is an oxide layer (line 19, Col. 5).

Regarding claim 25, Hong et al. discloses the second oxide layer is TEOS oxide layer (lines 8-11, Col. 3).

Regarding claim 26, Hong et al. discloses wherein the planarizing is chemical mechanical polishing (lines 25-26, Col. 5).

Regarding claim 27, Hong et al. discloses a method of forming a trench isolation similar to what recited in claim 27 (See Figs. 1-5 and Cols. 1-8), the method comprising:

. providing a semiconductor substrate 10, wherein a pad layer 11, a mask layer (line 47, col. 3), and a patterned photoresist layer (not shown, line 49, Col. 3) with an opening are formed thereon;

. etching the mask layer, the pad layer, and the substrate to form a trench 19 using patterned photoresist layer as a mask (lines 50-53, Col. 3);

. removing the patterned photoresist layer (Fig. 1);

. forming an oxide layer 21 to cover the substrate and the trench wherein the trench is filled with the first insulating layer (fig. 2), the oxide layer can be formed using LPCVD (Cols. 1-2);

. anisotropically etching the first insulating layer (lines 65-67, Col. 4) to below the level of the semiconductor substrate (211, fig. 3);

. forming an insulating layer 31 to cover the substrate and the trench, and planarizing the second insulating layer to expose the mask layer (lines 25-28, Col. 5);

. removing the mask layer (Fig. 5).

Hong et al. fails to disclose the formation of spacer on a sidewall of the trench by etching the first insulating layer.

Lin et al. discloses the method of filling trench isolation similar to Hong et al. and further discloses the formation of spacer on a sidewall of the trench by etching the first insulating layer. It would have been obvious to one having ordinary skill in the art at the time the invention was made to etch the first insulating layer as disclosed in Hong et al. or a spacer as disclosed in Lin et al. because the functions and manners of the device would not make any different in the method of forming trench isolation having high aspect ratio using two steps of filling the trench.

Regarding claim 28, Hong et al. discloses wherein the pad layer is an oxide layer.

Regarding claim 29, Hong et al. discloses the mask layer is a nitride layer (lines 28-29, Col. 5).

Regarding claim 31, Hong et al. discloses the etching process can be anisotropic etching but fails to specify that the anisotropic etching is plasma or reactive ion etching. It would have been well known in the art that plasma or reactive ion etching is one type of anisotropic etching.

Regarding claim 32, Hong et al. discloses the oxide layer is etched to have a surface is lower than the substrate.

Regarding claim 33, Hong et al. discloses the insulating layer is an oxide layer (line 19, Col. 5).

Regarding claim 34, Hong et al. discloses the insulating layer is TEOS oxide layer.

Regarding claim 35, Hong et al. discloses wherein the planarizing is chemical mechanical polishing (lines 25-26, Col. 5).

9. **Claim 30 is rejected under 35 U.S.C. 103 (a) as being unpatentable over Hong et al., U.S. Patent No. 6,566,229, in view of Lin et al., U.S. patent No. 6,713,365, and further in view of Hong et al., U.S. Patent No. 6,593,207.**

Regarding claim 30, Hong et al., U.S. Patent No. 6,566,229 doesn't mention the aspect ratio of the trench is greater than 6, however, Hong et al., U.S. Patent No. 6,593,207 discloses that the aspect ratio of the trench is 4 or higher (lines 42-43, Col. 4). It would have been obvious to one having ordinary skill in the art at the time the invention was made to have high aspect ratio is greater than 6 because when the high aspect ratio is high, the trench is not able to be filled in one step for forming a device isolation but two steps are required as disclosed in Hong et al. and present invention.

10. Claims 36-41 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Hong et al., U.S. Patent No. 6,566,229, in view of Hong et al., U.S. Patent No. 6,593,207.

Regarding claim 36, Hong et al. discloses a method of forming a trench isolation similar to what recited in claim 36 (See Figs. 1-5 and Cols. 1-8), the method comprising:

providing a semiconductor substrate 10, wherein a pad layer 11, a mask layer (line 47, col. 3), and a patterned photoresist layer (not shown, line 49, Col. 3) with an opening are formed thereon;

. etching the mask layer, the pad layer, and the substrate to form a trench 19 using patterned photoresist layer as a mask (lines 50-53, Col. 3);

. removing the patterned photoresist layer (Fig. 1);

. forming an oxide layer 21 to cover the substrate and the trench wherein the trench is filled with the first insulating layer (fig. 2), the oxide layer can be formed using LPCVD (Cols. 1-2);

. anisotropically etching the first insulating layer (lines 65-67, Col. 4) to below the level of the semiconductor substrate (211, fig. 3) by at least 300 A (about 1000 A; line 65, Col. 4);

. forming an insulating layer 31 to cover the substrate and the trench, and planarizing the second insulating layer to expose the mask layer (lines 25-28, Col. 5);

. removing the mask layer (Fig. 5).

Hong et al., U.S. Patent No. 6,566,229 doesn't mention the aspect ratio of the trench is greater than 6, however, Hong et al., U.S. Patent No. 6,593,207 discloses that the aspect ratio of the trench is 4 or higher (lines 42-43, Col. 4). It would have been obvious to one having ordinary skill in the art at the time the invention was made to have high aspect ratio is greater than 6 because when the high aspect ratio is high, the trench is not able to be filled in one step for forming a device isolation but two steps are required as disclosed in Hong et al. and present invention.

Regarding claim 37, Hong et al. discloses wherein the pad layer is an oxide layer.

Regarding claim 38, Hong et al. discloses the mask layer is a nitride layer (lines 28-29, Col. 5).

Regarding claim 39, Hong et al. discloses the etching process can be anisotropic etching but fails to specify that the anisotropic etching is plasma or reactive ion etching. It would have been well known in the art that plasma or reactive ion etching is one type of anisotropic etching.

Regarding claim 40, Hong et al. discloses the insulating layer is TEOS oxide layer (lines 8-11, Col. 3).

Regarding claim 41, Hong et al. discloses wherein the planarizing is chemical mechanical polishing (lines 25-26, Col. 5).

11. Claims 42-48 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Hong et al., U.S. Patent No. 6,566,229, in view of Hong et al., U.S. Patent No. 6,593,207, and further in view of Lin et al., U.S. Patent No. 6,713,365.

Regarding claim 42, Hong et al. discloses a method of forming a trench isolation similar to what recited in claim 42 (See Figs. 1-5 and Cols. 1-8), the method comprising:

. providing a semiconductor substrate 10, wherein a pad layer 11, a mask layer (line 47, col. 3), and a patterned photoresist layer (not shown, line 49, Col. 3) with an opening are formed thereon;

. etching the mask layer, the pad layer, and the substrate to form a trench 19 using patterned photoresist layer as a mask (lines 50-53, Col. 3);

. removing the patterned photoresist layer (Fig. 1);

. forming an oxide layer 21 to cover the substrate and the trench wherein the trench is filled with the first insulating layer (fig. 2), the oxide layer can be formed using LPCVD (Cols. 1-2);

. anisotropically etching the first insulating layer (lines 65-67, Col. 4) to below the level of the semiconductor substrate (211, fig. 3) by at least 300 A (about 1000 A; line 65, Col. 4);

. forming an insulating layer 31 to cover the substrate and the trench, and planarizing the second insulating layer to expose the mask layer (lines 25-28, Col. 5);

. removing the mask layer (Fig. 5).

Hong et al., U.S. Patent No. 6,566,229 doesn't mention the aspect ratio of the trench is greater than 6, however, Hong et al., U.S. Patent No. 6,593,207 discloses that the aspect ratio of the trench is 4 or higher (lines 42-43, Col. 4). It would have been obvious to one having ordinary skill in the art at the time the invention was made to have high aspect ratio is greater than 6 because when the high aspect ratio is high, the trench is not able to be filled in one step for forming a device isolation but two steps are required as disclosed in Hong et al. and present invention.

Hong et al. fails to disclose the formation of spacer on a sidewall of the trench by etching the first insulating layer.

Still regarding claim 42, Lin et al. discloses the method of filling trench isolation similar to Hong et al. and further discloses the formation of spacer on a sidewall of the trench by etching the first insulating layer. It would have been obvious to one having ordinary skill in the art at the time the invention was made to etch the first insulating layer as disclosed in Hong et al. or a spacer as disclosed in Lin et al. because the functions and manners of the device would not make any different in the method of forming trench isolation having high aspect ratio using two steps of filling the trench.

Regarding claim 43, Hong et al. discloses wherein the pad layer is an oxide layer.

Regarding claim 44, Hong et al. discloses the mask layer is a nitride layer (lines 28-29, Col. 5).

Regarding claim 45, Hong et al. discloses the etching process can be anisotropic etching but fails to specify that the anisotropic etching is plasma or reactive ion etching. It would have been well known in the art that plasma or reactive ion etching is one type of anisotropic etching.

Regarding claim 46, Hong et al. discloses that after etching, the oxide layer is below the substrate.

Regarding claim 47, Hong et al. discloses the insulating layer is TEOS oxide layer (lines 8-11, Col. 3).

Regarding claim 48, Hong et al. discloses wherein the planarizing is chemical mechanical polishing (lines 25-26, Col. 5).

12. If Applicants are aware of better art than that which has been cited, they are required to call such to attention of the examiner.

13. When responding to the office action, Applicants' are advice to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

Conclusion

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao P. Le whose telephone number is 571-272-1785. The examiner can normally be reached on M-T (7-6).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thao P. Le
Examiner
Art Unit 2818